WAFER SCALE HIGH DENSITY PROBE ASSEMBLY, APPARATUS FOR USE THEREOF AND METHODS OF FABRICATION THEREOF

This application claims priority from Provisional Application U.S. Serial No. 60/026,088 which was filed on September 13, 1996.

CROSS REFERENCE TO RELATED APPLICATION

The teaching of U.S. Application Serial No. _____ filed on the same day herewith entitled, "INTEGRATED COMPLIANT PROBE FOR WAFER LEVEL TEST AND BURNIN" to Brian S. Beaman et al. and the teaching of U.S. Application Serial No. _____ filed on the same day herewith entitled, "PROBE STRUCTURE HAVING A PLURALITY OF DISCRETE INSULATED PROBE TIPS PROJECTING FROM A SUPPORT SURFACE, APPARATUS FOR USE THEREOF AND METHODS OF FABRICATION THEREOF" to Brian S. Beaman et al. is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention is directed to structures useful as probes for testing of electrical interconnections to integrated circuit devices and other electronic components and particularly to testing of integrated circuit devices with rigid interconnection pads and multi-chip module packages with high density interconnection pads.

BACKGROUND OF THE INVENTION

Integrated circuit (IC) devices and other electronic components are normally tested to verify the electrical function of the device and certain devices require high temperature burn-in testing to accelerate early life failures of these devices. Wafer probing is typically done on a single chip site at temperatures ranging

from 25C - 125C while burn-in is typically done on diced and packaged chips at temperatures ranging from 80C to 140C. Wafer probing and IC chip burn-in at elevated temperatures of up to 200C has several advantages and is becoming increasingly important in the semiconductor industry. Simultaneous testing of multiple chips on a single wafer has obvious advantages for reducing costs and increasing production thruput and is a logical step towards testing and burn-in of an entire wafer.

The various types of interconnection methods used to test these devices include permanent, semi-permanent, and temporary attachment techniques. The permanent and semi-permanent techniques that are typically used include soldering and wire bonding to provide a connection from the IC device to a substrate with fan out wiring or a metal lead frame package. The temporary attachment techniques include rigid and flexible probes that are used to connect the IC device to a substrate with fan out wiring or directly to the test equipment.

The permanent attachment techniques used for testing integrated circuit devices such as wire bonding to a leadframe of a plastic leaded chip carrier are typically used for devices that have low number of interconnections and the plastic leaded chip carrier package is relatively inexpensive. The device is tested through the wire bonds and leads of the plastic leaded chip carrier and plugged into a test socket. If the integrated circuit device is defective, the device and the plastic leaded chip carrier are discarded.

The semi-permanent attachment techniques used for testing integrated circuit devices such as solder ball attachment to a ceramic or plastic pin grid array package are typically used for devices that have high number of interconnections and the pin grid array package is relatively expensive. The device is tested through the solder balls and the internal fan out wiring and pins of the pin grid array package that is plugged into a test socket. If the integrated circuit device is defective, the device can be removed from the pin grid array package by heating the solder balls to their melting point. The processing cost of heating

and removing the chip is offset by the cost saving of reusing the pin grid array package.

The most cost effective techniques for testing and burn-in of integrated circuit devices provide a direct interconnection between the pads on the device to a probe sockets that is hard wired to the test equipment. Contemporary probes for testing integrated circuits are expensive to fabricate and are easily damaged. The individual probes are typically attached to a ring shaped printed circuit board and support cantilevered metal wires extending towards the center of the opening in the circuit board. Each probe wire must be aligned to a contact location on the integrated circuit device to be tested. The probe wires are generally fragile and easily deformed or damaged. This type of probe fixture is typically used for testing integrated circuit devices that have contacts along the perimeter of the device. This type of probe is also much larger than the IC device that is being tested and the use of this type of probe for high temperature testing is limited by the probe structure and material set.

Another technique used for testing IC devices comprises a thin flex circuit with metal bumps and fan out wiring. The bumps are typically formed by photolithographic processes and provide a raised contact for the probe assembly. The bumps are used to contact the flat or recessed aluminum bond pads on the IC device. An elastomer pad is typically used between the back of the flex circuit and a pressure plate or rigid circuit board to provide compliance for the probe interface. This type of probe is limited to flexible film substrate materials that typically have one or two wiring layers. Also, this type of probe does not provide a wiping contact interface to ensure a low resistance connection.

The aluminum bond pads on a high density IC device are typically rectangular in shape and are recessed slightly below the surface of the passivation layer. If the wiping action of the high density probe is not controlled, the probe contact may move in the wrong direction and short to an adjacent aluminum bond pad or

the probe contact may move off of the aluminum bond pad onto the surface of the passivation layer and cause an open connection.

Gold plated contacts are commonly used for testing and burn-in of IC devices. The high temperature test environment can cause diffusion of the base metal of the probe into the gold plating on the surface. The diffusion process creates a high resistive oxide layer on the surface of the probe contact and reduces the probe life.

The position of the probe tips must be controlled to ensure accurate alignment of the probes to the interconnection pads on the IC device. During high temperature burn-in testing, the thermal expansion mismatch between the probe structure and the IC device must be small to ensure that the probe position does not vary significantly over the burn-in temperature range. Thermal expansion mismatch within the probe structure can result in contact reliability problems.

The challenges of probing a single high density integrated circuit device are further multiplied for multi-chip and full wafer testing applications. Probe fabrication techniques and material selection are critical to the thermal expansion and contact alignment considerations. A small difference in the thermal expansion of the substrate, wafer, and probe construction will cause misalignment of the probe tip to the wafer contact pad. Compliance of the probe structure is another critical factor. Slight variations in the wafer metalization, warpage of the wafer, and slight variations in the probe height contribute to the total compliance requirements for the probe structure.

US Patent 5,177,439, issued January 5, 1993 to Liu et al., is directed to fixtures for testing bare IC chips. The fixture is manufactured from a silicon wafer or other substrate that is compatible with semiconductor processing. The substrate is chemically etched to produce a plurality of protrusions to match the I/O pattern on the bare IC chip. The protrusions are coated with a conductive material and connected to discrete conductive fanout wiring paths to allow connection to an

external test system. The probe geometry described in this patent does not provide a compliant interface for testing the aluminum bond pads on the IC device and does not provide a wiping contact interface. The substrate used for fabrication of this probe fixture is limited to semiconductor wafers which are relatively expensive. The high density probe with controlled wipe can be fabricated on a variety of inexpensive substrate with the fanout wiring.

IBM Docket #YO993028 describes a high density test probe for integrated circuit devices. The probe structure described in this docket uses short metal wires that are bonded on one end to the fan out wiring on a rigid substrate. The wires are encased in a compliant polymer material to allow the probes to compress under pressure against the integrated circuit device. The wire probes must be sufficiently long and formed at an angle to prevent permanent deformation during compression against the integrated circuit device. The probe structure described in this patent does not provide a means of controlling the direction and length of the wiping action of the contact interface.

IBM Docket #YO995-113 describes a high density test probe for integrated circuit devices with aluminum bond pads. The probe structure described in this patent does is subject to contact reliability problems due to the thermal expansion mismatch between the metal wire conductor and the elastomer material surrounding the wires. At high temperatures, the elastomer material expands sufficiently to cause an open connection between the metal wire probes and the IC bond pads. Also, after repeated thermal cycles, the ends of the probe wires are sufficiently exposed above the surface of the elastomer material to be deformed during a subsequent contact cycle with the bond pads on an IC device.

OBJECTS

It is the object of the present invention to provide a probe for testing integrated circuit devices and other electronic components that use bond pads for the

interconnection means.

Another object of the present invention is to provide a probe structure that is an integral part of the fan out wiring on the test substrate or other printed wiring means to minimize the electrical conductor length as well as the contact resistance of the probe interface.

A further object of the present invention is to provide a probe with a compliant interface to compensate for slight variations in the rigid bond pad heights on the IC device and variations in the height of the probe contacts.

An additional object of the present invention is to provide a raised probe tip for contacting recessed surfaces on the IC device.

Yet another object of the present invention is to provide a probe with a wiping contact interface where the direction and length of the contact wipe is controllable.

Yet a further object of the present invention is to provide a probe construction that has thermal expansion characteristics that are matched to the IC device to be tested or burned-in at high temperature.

Yet an additional object of the present invention is to provide a probe construction that has high durability and reliability for repeated thermal and mechanical cycling.

Yet another object of the present invention is to provide a probe structure that can be used for single chip or multiple chip wafer testing.

SUMMARY OF THE INVENTION

A broad aspect of the present invention is a structure having a substrate having a surface; a plurality of elongated electrical conductors extending away from the surface; each of the elongated electrical conductors having a first end affixed to said surface and a second end projecting away from the surface; there being a plurality of the second ends; and a means for permitting each of the plurality of second ends to move about reference positions.

According to a more specific aspect of the structure according to the present invention is the means for permitting is a sheet of material having a plurality of opening therein through which the second ends project, therebeing a perforation in the sheet in the vicinity of said openings permitting the second ends to move when the structure is used to electrically probe an electronic device.

According to a more specific aspect of the present invention the perforation are a plurality independent perforations about each of said through-hole.

According to a more specific aspect of the present invention the plurality of interconnected perforations about each of said through-holes.

According to another broad aspect of the present invention the structures according to the present invention are incorporated into an apparatus to test an electronic device having a means for holding the structure of 1, means for retractably moving the structure 1 towards and away from the electronic device so that the second ends contact electrical contact locations on said electronic device, and means for applying electrical signals to the elongated electrical conductors.

Another broad aspect of the present invention as a method of providing a substrate having a surface; forming a plurality of elongated electrical conductors extending away from the surface; each of the elongated electrical conductors

having a first end fixed to the surface and a second end projecting away from the surface; there being a plurality of said second ends; and providing a means for permitting each of the plurality of second ends to move about reference positions.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become apparent upon further consideration of the following detailed description of the invention when read in conjunction with the drawing figures, in which:

FIGURE 1 shows a cross section of an integrated cantilever compliant test probe attached to a substrate and pressed against the aluminum bond pads on an integrated circuit device.

FIGURE 2 is essentially the same as FIGURE 1 with a modified arrangement of the cantilevered flap.

FIGURES 3-6 show the processes used to fabricate the integrated cantilever test probe on a fan out wiring substrate.

FIGURE 7 shows an alternate process used to fabricate the integral cantilever compliant test probe.

FIGURE 8 shows a top view of the preferred embodiment of a integrated cantilever compliant test probe.

FIGURE 9 shows a top view of the preferred embodiment of the integral cantilever compliant test probe with a modified cantilevered flap configuration to allow the probes to be fabricated with a closer spacing.

FIGURE 10 shows a cross section of an embodiment of the integrated cantilever

compliant test probe attached to a substrate and pressed against the aluminum bond pads on an integrated circuit device.

FIGURE 11 shows a top view of an embodiment of the integrated cantilever compliant test probe.

FIGURE 12 shows a cross section of an embodiment of the integrated cantilever complaint test probe attached to a substrate and pressed against the aluminum bond pads on an integrated circuit device.

FIGURE 13 shows a top view of an embodiment of the integrated cantilever compliant test probe.

FIGURE 14 shows a cross section of an embodiment of the integrated cantilever compliant test probe.

FIGURE 15 shows a cross section of an integrated cantilever compliant test probe array for testing multiple IC devices on a single wafer.

FIGURE 16 shows a top view of an integrated cantilever compliant test probe array for testing all of the IC devices on a single wafer.

FIGURE 17 shows various shapes to the elongated conductors such as "S" shaped, curved, piece wire linear or combination thereof.

FIGURE 18 shows spring means for maintaining sheet (20) resiliently spaced apart from surface (12) of substrate (11). The resilient spacers can be springs or are elastomeric material.

FIGURE 19 shows a schematic diagram of a probing apparatus incorporating the probe structures of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Preferred Embodiment

FIGURE 1 shows a cross section of a test substrate (11) and an integrated cantilever compliant test probe (10) according to the present invention. The test substrate (11) provides a rigid base for attachment of the probes (10) and fan out wiring from the high density array of probe contacts to a larger grid of pins or other interconnection means to the equipment used to electrically test the integrated circuit device. The fan out substrate can be made from various materials and constructions including single and multi-layer ceramic with thick or thin film wiring, silicon wafer with thin film wiring, or epoxy glass laminate construction with high density copper wiring. The test probes (10) are attached to the first surface (12) of the substrate (11). The probes are used to contact the bond pads (31), typically aluminum bond pads, on the electronic device, typically an integrated circuit device (30). The bond pads (31) are typically recessed slightly below the surface of the passivation layer (32) of the electronic device (30). The geometry of the integrated cantilever compliant test probe (10) is optimized to provide a wiping contact interface to penetrate the oxides on the surface of the bond pads (31) to provide a low resistance connection.

FIGURE 2 is essentially the same as FIGURE 1 with a modified arrangement of the cantilevered flap in the polymer material. The test probe (10) is attached directly to the fan out wiring (13) on the first surface (12) of the substrate (11) to minimize the resistance of the probe interface. The probe geometry is optimized to provide a flexible contact interface that controls the direction and length of the wiping action. The elastomer material (17) preferably surrounding the probes provides an compliant structure and the cantilevered flaps (23) in the thin polymer sheet (18) are used to the controls the direction and length that the probe tip (16) can wipe against the aluminum bond pads (31) on the IC device (30). The probe tip (16) is bonded to the cantilevered flap (23) using a suitable epoxy material (22). As the high density probe (10) is pressed against the IC

device (30), the probe wire (15) and the cantilevered flap (23) rotate and the probe tip (16) slides along the surface of the bond pads (31) of the IC device (30). The probe tip ends (16) move about a reference position that is the position probe tip ends have when the probe tip ends are not pressed against a device under test.

The length of the sliding or wiping action is restricted by the angle and length of the probe wire (15) and the length of the cantilevered flap (23) in the sheet (20). Sheet (20) is preferably of a polymer material.

FIGURE 3 shows a process used to fabricate the integrated cantilever compliant test probe. A thermosonic wire bonder tool is used to attach ball bonds (14) to the fan out wiring (13) on the first surface (12) of the rigid substrate (11). The wire bonder tool uses a first ceramic capillary (40) to press the ball shaped end of the bond wire (41) against the first surface (12) of the substrate (11). Compression force and ultrasonic energy are applied through the first capillary (40) tip and thermal energy is applied from the wire bonder stage through the substrate (11) to bond the ball shaped end of the bond wire (41) to the fan out wiring (13) on the first surface (12) of the substrate (11). The bond wire (41) is positioned at an angle and a shear blade (42) is used to sever the bond wire (41) to create an angled segment of wire (15) protruding vertically from the ball bond (14). The movement of the ceramic capillary (40) is controlled during this process to provide a short straight section of the wire (43) that is perpendicular to the surface of the rigid substrate (10).

FIGURE 4 shows a laser (50) (preferably an argon ion laser) used to melt the ends of the short straight sections of the wire (15) to create a ball shaped contact (16). The smooth surface of the ball shaped contact (16) is ideal for a wiping interface. The size of the ball shaped contact (16) on the end of the probe is controlled by the laser power density and the alignment of the focal point from the tip of the straight wire section (43). The shape at the end of the wire can be any shaped protuberance such as, for example, a ball with a barbed or pointed end or a shaft pointed end.

FIGURE 5 shows a casting dam (60) placed around the array of high density probes. The casting dam (60) is used to contain the liquid elastomer (61) until it is cured. A controlled volume of liquid elastomer resin (61) is dispensed into the cavity and allowed to settle out before curing. The height of the elastomer material (61) is controlled so that ball shaped end of the probe (16) is slightly above the surface of the elastomer (61). Once the elastomer has cured, the casting dam (60) is removed and a sheet (20) with cantilever flats (23) and corresponding openings is placed over the ball shaped ends (16) of the probes as shown in FIGURE 6. The sheet (20) is preferably a polymer sheet. An epoxy material (22) is applied to the openings in the polymer sheet (20) and cured to bond the probe to the cantilevered flaps (23).

FIGURE 7 shows another process according to the present invention used to fabricate the integral cantilever compliant test probe (100). The sequence of the fabrication process is changed in order to cast and cure the elastomer resin before the laser ball forming process. After the elastomer (17) is cast and cured, a thin polymer sheet (20) with small opening (28) corresponding to the probe locations is place over the straight ends of the probe wires (43). A (preferably thin metal) mask (51) with larger openings (52) corresponding to the probe locations is also placed over the ends of the probe wires (43). After the (preferably argon-ion) laser (50) is used to form the ball shaped (16) ends on the probe wires, the metal mask (51) is removed from the top surface of the probe structure (100). The mask (51) prevents polymer sheet (20) from being exposed to the light of laser (50). The mask (51) can be of any light blocking material such as metal, ceramic, glass, polymer and combinations thereof.

FIGURE 8 shows a top view of the test probe and the cantilevered flaps (23) in the sheet (20) that is attached to the top of the layer of elastomer material (17). Openings (21) in the sheet (20) are aligned with the ball shaped ends (16) of the probes and preferably bonded to the polymer sheet using an epoxy material. The accuracy of the location of the ball shaped probe contacts (16) is determined by the accuracy of the location of the openings (21) in the polymer

sheet (20). The sheet (20) material is preferably selected to match the thermal coefficient of expansion (TCE) of the device or other substrate material of the device to be tested at elevated temperatures. Flap (23) is formed by perforation (24) which is "U" shaped in FIGURE 8. Perforation (24) can be any shape such as triangular, a section of a circle, rectangular, polygonal and combinations thereof.

FIGURE 9 shows a top view of an embodiment of the integral cantilever compliant test probe with a modified cantilevered flap (23) configuration to allow the probes to be fabricated with a closer spacing. Other configurations of the cantilever flap are possible to optimize the compliance and spacing requirements of the probe array. Flap (23) if formed by perforation (25) which is a perforation interconnected about a group of openings (22).

FIGURE 10 shows another embodiment of the integrated cantilever compliant test probe (80). Instead of bonding the probe wire (15) to the cantilevered flaps (23) in the material (20), the embodiment (80) uses a slotted opening (26) in the cantilevered flaps (23) to control the movement of the probe tip (16). The width of the slot (26) in the cantilevered flap (23) is slightly wider than the diameter of the probe wire (15). The narrow width of the slot (26) prevents the ball shaped probe tip (16) from sinking into the soft elastomer material (17) during compression of the probe structure. FIGURE 11 shows a top view of the embodiment of FIGURE 10. Again perforation (29) is shown "U" shaped but can be any shape.

FIGURES 12 and 13 show another embodiment of the integrated cantilever compliant test probe (90). The structure of the embodiment (90) is similar to the embodiment (80) of the test probe of FIGURES 10 and 11. The spacing between the probes in one direction is much farther apart than in the opposite direction. The embodiment (90) uses a single cantilevered flap (27) to control several probe wires. Perforation (22) partially surrounds a group of openings or slots (26).

FIGURE 14 shows another embodiment of the test probe (70). The embodiment (70) of the test probe does not use a cantilevered flap and the end of the probe (16) is restricted by the collars (25) surrounding each of the probe wires (15). The collars (25) are positioned below the ball shaped ends of the probe tips (16) to prevent the tips (16) from sinking into the soft elastomer material (17) during compression. The collars (25) sit in separate openings (24) in the sheet (20) and allow vertical movement of the probe tips (16) but restrict lateral movement.

FIGURE 15 shows a cross section of an integrated cantilever compliant test probe array (100) for testing multiple IC devices on a single wafer. The integrated test probe (100) shown in figure 15 includes four distinct probe arrays used to test individual IC devices on the wafer (130). The construction of each distinct probe array is identical to that shown in figure 1, but can be any of the embodiments described herein or in the US patent applications and patents incorporated herein by reference. The substrate (110) used as the base for building the test probe has an array of pads (113) on the top surface (112) that matches the pattern of contacts (131) on the wafer (130) to be tested. The test probes are bonded to these pads (113) and formed at an angle or other suitable shape as described in the FIGURES 3 to 6 and 17. The angle or shape of the bond wires (115) are preferably all be the same to ensure accurate positioning of the ball shaped contact (116) on the end of the probe. Likewise, the geometry of the cantilevered sections (118) of the top polymer sheet (120) must be identical to ensure accurate alignment and uniform wiping against the mating contact pads (131) on the wafer (130). Uniform material properties and height of the elastomer material (117) are necessary to provide optimum compliance and contact normal force across the entire surface of the probe array.

FIGURE 16 shows a top view of an integrated cantilever compliant test probe array (100) for testing all of the IC devices on a single wafer (130). The integrated test probe (100) shown in figure 16 includes twelve distinct probe arrays used to test all of the IC devices on the wafer (130). The outline of the wafer (130) and the individual IC devices (132) are shown with broken or dashed

lines. The location of each array of probes corresponds with the pads on each of the individual IC devices (132) on the wafer (130). The location of the ball shaped ends (118) of the test probes is controlled by the location of the opening in the cantilevered sections (118) of the thin polymer sheet (120).

FIGURE 17 schematically shares a variety of shape of probe wires useful to practice the present invention, such as "S" showed "C" shaped, continuously curved, piece wire curved, piece wire linear and combinations thereof.

FIGURE 18 schematically shows alternative embodiments of compliant frame structures (17) to support probe tip positioning structure (20) to be maintaining in position and to move as the probe tip ends (16) move when they are moved into engagement with electronic device pads (31).

FIGURE 19 schematically shows an apparatus for moving probe structure 10 towards and away from electronic device 204 so that probe tips 210 engage and disengage electrical contact locations 212 on electronic device 204. Probe 10 is mounted on to holder 200 having means 214 for applying electric power to the probe tips 210. Electronic device 206 is held on base 206. Holder 200 is physically connected to support 202 which is converted to arm 208 which is converted to base 206. Support 202 is adapted for up and down movement. Examples of an apparatus to provide the means for support and up and down movement can be found in US Patent 5,439,161 and US Patent 5,132,613, the teachings of which are incorporated herein by reference.

The teaching of the following patent co-pending applications are incorporated herein by reference:

U.S. Patent 5,371,654 entitled, "THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION PACKAGE";

U.S. Patent Application Serial No. 08/614,417 entitled, "HIGH DENSITY CANTILEVERED PROBE FOR ELECTRONIC DEVICES"* (Now pat No. 5811982);

U.S. Patent Application Serial No. 08/641,667 entitled, "HIGH DENSITY TEST PROBE WITH RIGID SURFACE STRUCTURE"; PAT NO. 5,785,538

U.S. Patent Application Serial No. 08/527,733 entitled, "INTERCONNECTOR WITH CONTACT PADS HAVING ENHANCED DURABILITY"; Pat No. 5810607

U.S. Patent Application Serial No. 08/752,469 entitled, "FOAMED ELASTOMERS FOR WAFER PROBING APPLICATIONS AND INTERPOSER CONNECTORS";

U.S. Patent Application Serial No. 08/744,903 entitled, "INTEGRAL RIGID CHIP TEST PROBE"; PAT NO. 5838160

U.S. Patent Application Serial No. 08/756,831 entitled, "HIGH TEMPERATURE CHIP TEST PROBE"; (abandoned)

U.S. Patent Application Serial No. 08/756,830 entitled, "A HIGH DENSITY INTEGRAL TEST PROBE AND FABRICATION METHOD"; abandoned 28X

U.S. Patent Application Serial No. 08/754,869 entitled, "HIGH DENSITY INTEGRATED CIRCUIT APPARATUS, TEST PROBE AND METHODS OF USE THEREOF". PAT 5821763

It is to be understood that the above described embodiments are simply illustrative of the principles of the invention. Various other modifications and changes may be devices by those of skill in the art which will embody the principles of the invention and fall within the spirit and scope thereof.